

**EAST - [10772268.wsp:1]**

File View Edit Tools Window Help

☐ Drafts  
☐ Pending  
☒ Active  
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☒ L2: (914) (register near setting near method) or mode adj register adj set  
☐ Failed  
☐ Saved  
☐ Favorites  
☐ Tagged (0)  
☐ UDC  
☐ Queue  
☐ Trash

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	U	I	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	
1	<input type="checkbox"/>	<input type="checkbox"/>	US 20050108463 A1	20050519	17	System and method for multi-modal memory controller system operation	711/5	711/167	
2	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 20050105363 A1	20050519		Semiconductor memory device having column address path therein for reducing power consumption	365/222		
3	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 20050105362 A1	20050519		Semiconductor memory device for performing refresh operation	365/222		
4	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 20050105357 A1	20050519		Method and circuit configuration for refreshing data in a semiconductor memory	365/222		
5	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 20050099837 A1	20050512		Semiconductor memory device for controlling write recovery time	365/145		
6	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 20050097410 A1	20050505		Memory device and input signal control method of a memory device	714/718		
7	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 20050097292 A1	20050505		Synchronous memory device capable of controlling write recovery time	711/167		
8	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 20050094480 A1	20050505		Semiconductor memory and method for controlling the same	365/232		
9	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 20050088906 A1	20050428		Semiconductor memory device having different synchronizing timings depending on the value of CAS latency	365/233		
10	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 20050086037 A1	20050421		Memory device load simulator	703/14		
11	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 20050083217 A1	20050421		Method for transmitting and receiving signals in semiconductor device and semiconductor device therefor	341/53		

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